GOC-QF110 V1.1

Bluetooth Module Hardware Specification

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NOTES:

1.The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.
2.Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Date	Comments
V1.0	2019/03/30	Initial draft
V1.1	2020/01/09	Update pin definition

Contents

1. Introduction

GOC-QF110 is a Bluetooth module, audio and programmable application processor. It includes high-performance, analog, and digital audio codecs, speaker driver, advanced power management, and flexible interfaces including interintegrated circuit sound (PCM), universal asynchronous receiver transmitter (UART), and programmable input/output (PIO).

An application-dedicated Developer Processor and a system Firmware Processor run code from an external quad serial peripheral interface (QSPI) flash. Both processors have tightly coupled memory (TCM) and an on-chip cache for performance while executing from external flash memory. The system Firmware Processor provides functions developed by Goodocom Technologies Confidential, Ltd. The Developer processor provides flexibility to the product designer to customize their product.

The Audio subsystem contains a programmable Kalimba core running Goodocom Kymera system DSP architecture framework from read only memory (ROM). A range of audio processing capabilities are provided from ROM which are configurable in fully flexible audio graphs.

The flexibility provided by the programmable applications processor plus the ability to configure the audio processor enables manufacturers to easily differentiate products with new features.

GOC-QF110 is driven by a flexible, software platform with powerful integrated development environment (IDE) support.

1.1 Module Block Diagram

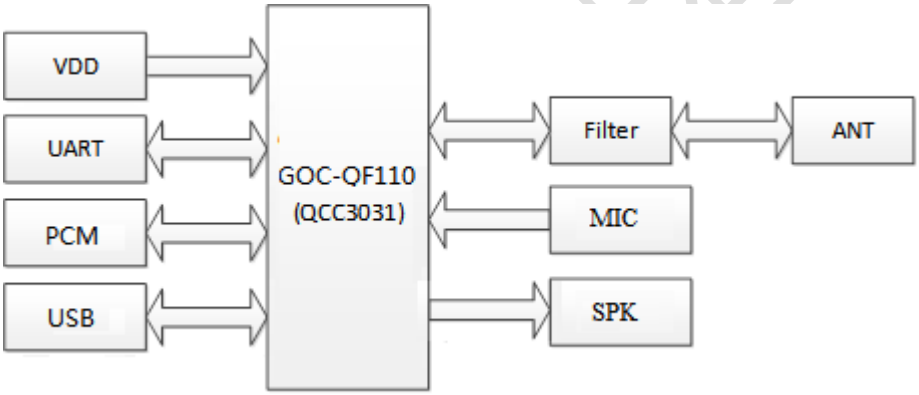

Figure 1: Module Block Diagram

1.2 Features

- High-performance programmable Bluetooth® stereo audio SoC with aptX audio
- Supports Bluetooth v5.0 including Bluetooth low energy 2 Mbps.
- Fully qualified single-chip dual-mode Bluetooth v5.0 system
- Tri-core processor architecture with low power for extended battery life
- Qualified to Bluetooth® v5.0 specification
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- 1-mic cVc™ speaker noise reduction and echo cancellation technology
- aptX, aptX HD, aptX Low Latency, SBC, and AAC audio codecs support
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy (Production parts)
- Bluetooth, Bluetooth low energy, and mixed topologies supported

- Class 3 support
- Programmable audio master clock (MCLK)
- Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:
  - SNR single-ended: 101 dB typ.
  - THD+N single-ended: -85 dB typ.
- A UART interface
- Green (restriction of hazardous substances (RoHS) compliant and no antimony or halogenated flame retardants)

1.3 Application

- Wireless speakers

2. Specification

Production	Bluetooth Module
Type	GOC-QF110
Standard	Bluetooth V5.0
IC	QCC3031
Frequency Range	2.402~2.480GHz ISM Band
Modulation Method	GFSK, π/4-DQPSK,8DPSK
Max speed for transfer	Asynchronous: 723.2kbps/57.6kbps Synchronous: 433.9kbps/433.9kbps
Hop	1600hops/sec, 1MHz channel space
Output impedance	50 ohms
Crystal Frequency	26MHz
Outer interface	UART, PCM, Speaker, Microphone
Apply to Bluetooth instructions	A2DP AVRCP HFP HSP SPP APTX
Range for working distance	10 meters
Receiving Sensitivity	-90dBm
Emissive power	<4dBm
Size	23.24mm *11.94mm *2.38mm.
Power Voltage	3.3V supply voltage
Storage temperature	-40℃ to +85℃
Temperature Range	-40℃ to +85℃
Humidity Range	10%~90% Non-Condensing

Table 1: Specification

3. Pin Diagram And Description

3.1 Pin Diagram

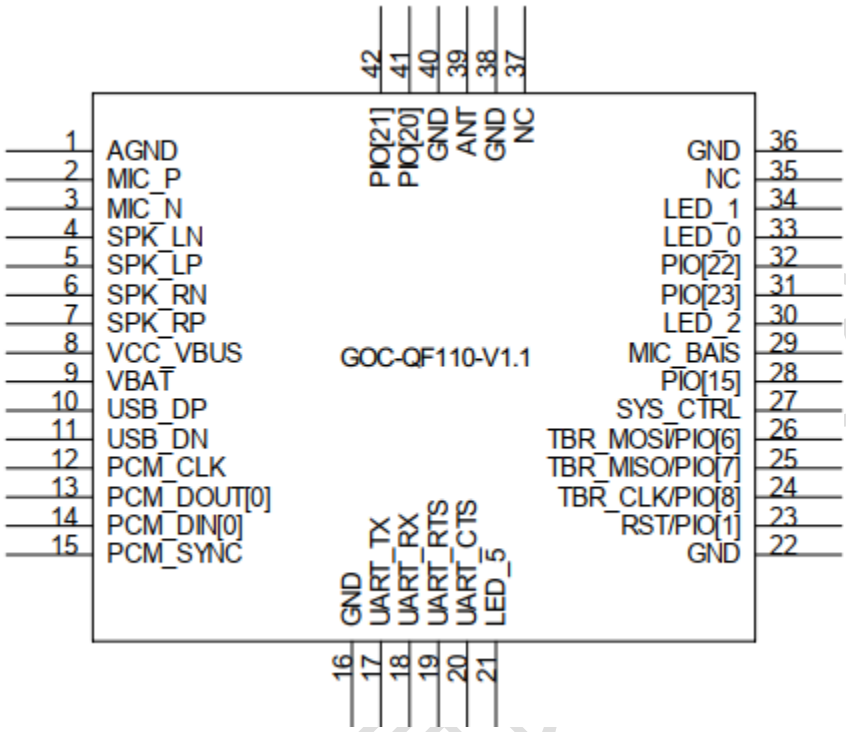

Figure 2: GOC-QF110 Pin Diagram

3.2 Pin Description

Pin	Pin Name	Pad Type	Description
1	AGND	AGND	Audio Ground
2	MIC_P	Input	Microphone differential input,positive
3	MIC_N	Input	Microphone differential input,negative
4	SPK_LN	Output	Headphone/speaker differential left output, negative
5	SPK_LP	Output	Headphone/speaker differential left output, positive
6	SPK_RN	Output	Headphone/speaker differential right output, negative
7	SPK_RP	Output	Headphone/speaker differential right output, positive
8	VCC_VBUS	Power	VCC_VBUS(USB Power input)
9	VBAT	Power	3.3V Supply Voltage
10	USB_DP	Digital	USB Full Speed device D+ I/O
11	USB_DN	Digital	USB Full Speed device D- I/O
12	PCM_CLK	Input/ Output	PCM_CLK
13	PCM_DOUT[0]	Output	PCM_DOUT
14	PCM_DIN[0]	Input	PCM_DIN
15	PCM_SYNC	Input/ Output	PCM_SYNC
16	GND	GND	Ground

17	UART_TX	Output	UART_TX
18	UART_RX	Input	UART_RX
19	UART_RTS	Input	UART_RTS
20	UART_CTS	Output	UART_CTS
21	LED_5	Input/ Output	General-purpose analog/digital input or open drain LED output
22	GND	GND	Ground
23	RST/PIO[1]	Input/ Output	RESET/Programmable I/O line 1
24	TBR_CLK/PIO[8]	Input/ Output	Alternative function: TBR_CLK/ Programmable I/O line 8
25	TBR_ MISO/PIO[7]	Input/ Output	Alternative function:TBR_MISO/ Programmable I/O line 7
26	TBR_ MOSI/PIO[6]	Input/ Output	Alternative function:TBR_MOSI/ Programmable I/O line 6
27	SYS_CTRL	Input	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation
28	PIO[15]	Input/Output	Programmable I/O line15
29	MIC_BAIS	Output	Mic bias output
30	LED_2	Input/ Output	General-purpose analog/digital input or open drain LED output
31	PIO[23]	Input/Output	Programmable I/O line23
32	PIO[22]	Input/Output	Programmable I/O line22
33	LED_0	Input/ Output	General-purpose analog/digital input or open drain LED output
34	LED_1	Input/ Output	General-purpose analog/digital input or open drain LED output
35	NC	NC	No connect
36	GND	GND	Ground
37	NC	NC	No connect
38	GND	GND	Ground
39	ANT	RF	Bluetooth transmit/receive
40	GND	GND	Ground
41	PIO[20]	Input/ Output	Programmable I/O line 20
42	PIO[21]	Input/ Output	Programmable I/O line 21

Table 2: Pin Description

3.3 PCB Layout Footprint

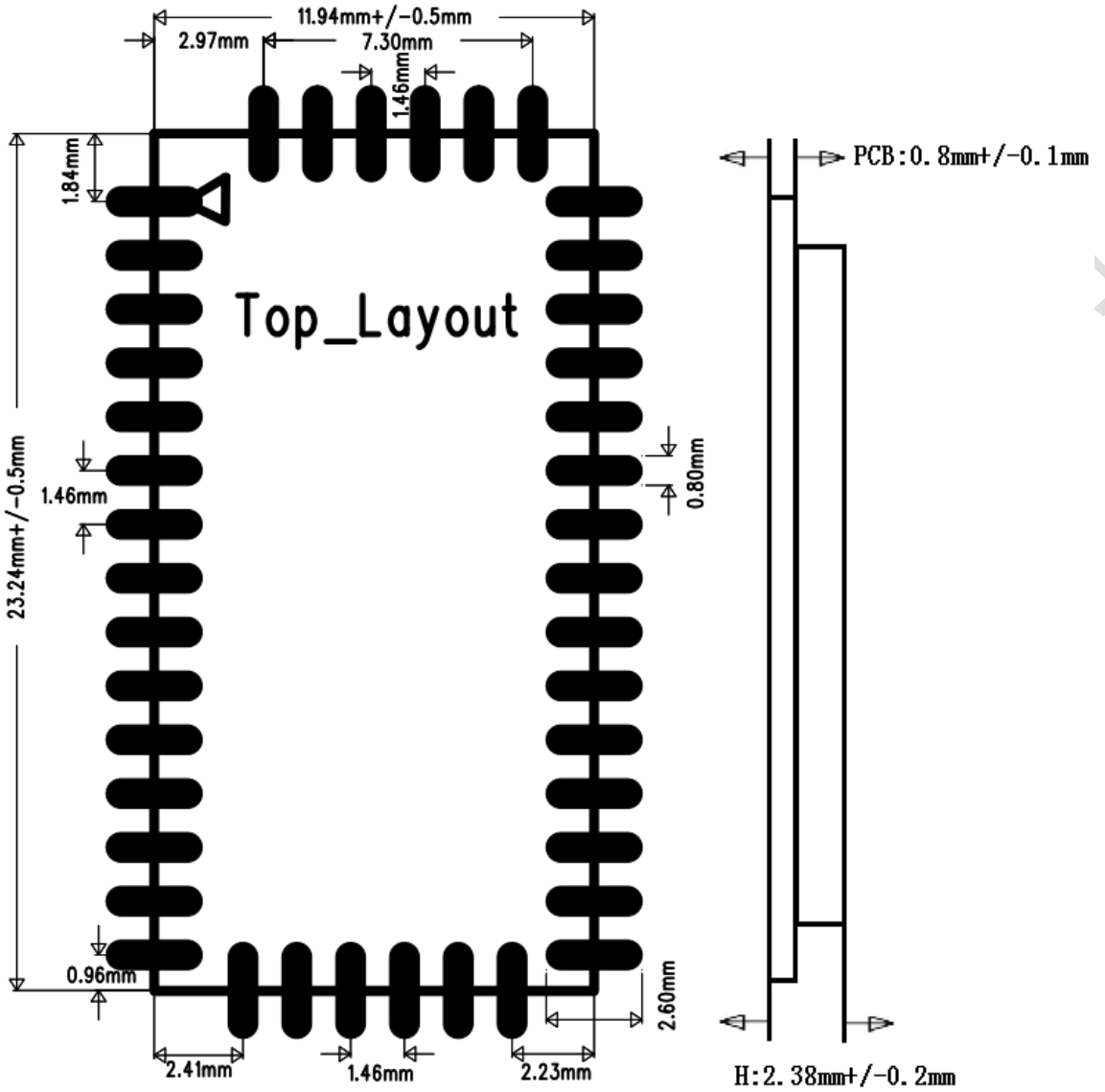

Figure 3: PCB Layout Footprint

4. System Power States

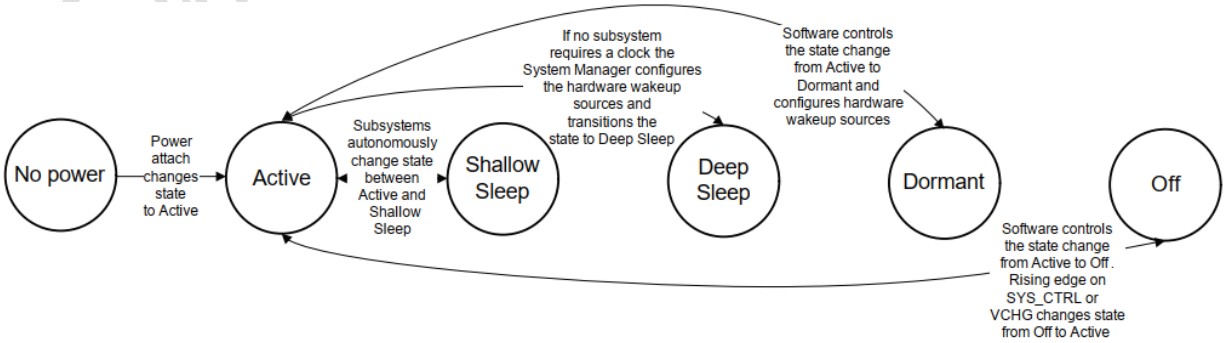

Figure 4: GOC-QF110 Static Power States Diagram

4.1 No Power State

When the GOC-QF110 has no power at all, it is in the No Power state. When power is present, for example on battery attach, the GOC-QF110 automatically boots and moves to Active state.

4.2 Active State

In Active state, the on-chip clocks and power supplies are running, and all functions of the IC are available.

4.3 Shallow Sleep State

Shallow Sleep state is functionally the same as the Active state. However, individual subsystems can autonomously enter Shallow Sleep state to conserve power. In Shallow Sleep state, a subsystem can turn off or reduce the frequency of clocks and/or power down memories.

4.4 Deep Sleep State

In Deep Sleep state, the main digital power rail (VDD_DIG_CORE) is in state retention. To reduce leakage the digital voltage is typically reduced to 0.85 V. The main digital clocks are stopped and a limited number of device features remain active, including:

■ Boot Manager
■ LED PWM drivers
■ PIO controller

GOC-QF110 extensively uses digital power islands. Deep Sleep state current varies significantly depending on which functions are active or in state retention.

The following events can move GOC-QF110 to Active state (selectable via software) from Deep Sleep state:

■ A rising edge on SYS_CTRL
■ A rising edge or a falling edge on VCHG
■ Activity on any PIO
■ Activity on any digital interface
■ A timer
■ Digital activity on any LED pads (when configured as a digital input)
■ Activity on the debug interfaces
■ USB device resume

4.5 Dormant State

In Dormant state, the PMU is enabled in an ultralow power mode. The main digital supply (VDD_DIG_CORE) is off.This configuration reduces power consumption but limits available device features.

In Dormant state, the following inputs can transition the IC to the Active state (selectable via software):

■ A rising edge on SYS_CTRL
■ A rising edge or a falling edge on VCHG
■ A timer

NOTE : Time accuracy in Dormant state is limited to ±20 %

4.6 Off State

The Off state is different to No Power state because the IC has power attached from VBAT. In this state the following events boot the chip and transition it to Active state:

■ A rising edge on SYS_CTRL held high for 20 ms
■ A rising edge on VCHG held high for 20 ms

NOTE : The device cannot power off with VCHG attached. Dormant state is the lowest possible power state

■ When voltage is present on the VCHG input.

4.7 Transition Between Static Power States

Transition into Shallow Sleep and Deep Sleep states is automatic, with the system constantly entering the lowest power mode. Transition into the Dormant and Off states is under the control of the application software.

4.8 Power Islands

To reduce digital leakage the Bluetooth, Audio, and Applications subsystems are contained within separate power islands. When these subsystems are enabled, the power is applied automatically

5. Host Interfaces Subsystem

GOC-QF110 provides a standard PCM interface capable of operating at up to a 192 kHz sample rate. The PCM port is highly configurable, and has the following options:

- ■ Master (generate CLK and SYNC) or Slave (receive CLK and SYNC)
- ■ Word Select polarity
- ■ Left or right justification
- ■ Sign extension / zero pad
- ■ Optional 1-bit period delay on WS to start of channel data
- ■ 13/16/24-bit per sample
- ■ Up to four slots per frame

NOTE:In multislot operation with 3 or 4 slots per frame, data padding to 32 bits within slots is not possible.

5.1 Host Interfaces Subsystem Features

supports the following Host Interfaces:

- ■ USB Device
- □ Full Speed (12 Mbps)
- □ Multiple IN and OUT endpoints, allocable individually
- □ Charging support
- ■ UART
- □ Supports H4 and BCSP HCI interfaces or raw UART to application

These host interfaces can operate concurrently, subject to pin multiplexing constraints, between the UART.

Host Interface signals for UART, SPI go via a PIO mux with a further multiplexing implemented at the top level to the PIOs. The Host Interface subsystem must be selected as the controlling subsystem for the relevant PIOs.

5.2 PCM Interface

GOC-QF110 provides a standard PCM interface capable of operating at up to a 192 kHz sample rate. The PCM port is highly configurable, and has the following options:

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NOTE In multislot operation with 3 or 4 slots per frame, data padding to 32 bits within slots is not possible.

5.2.1 PCM Master Mode Timing Diagram

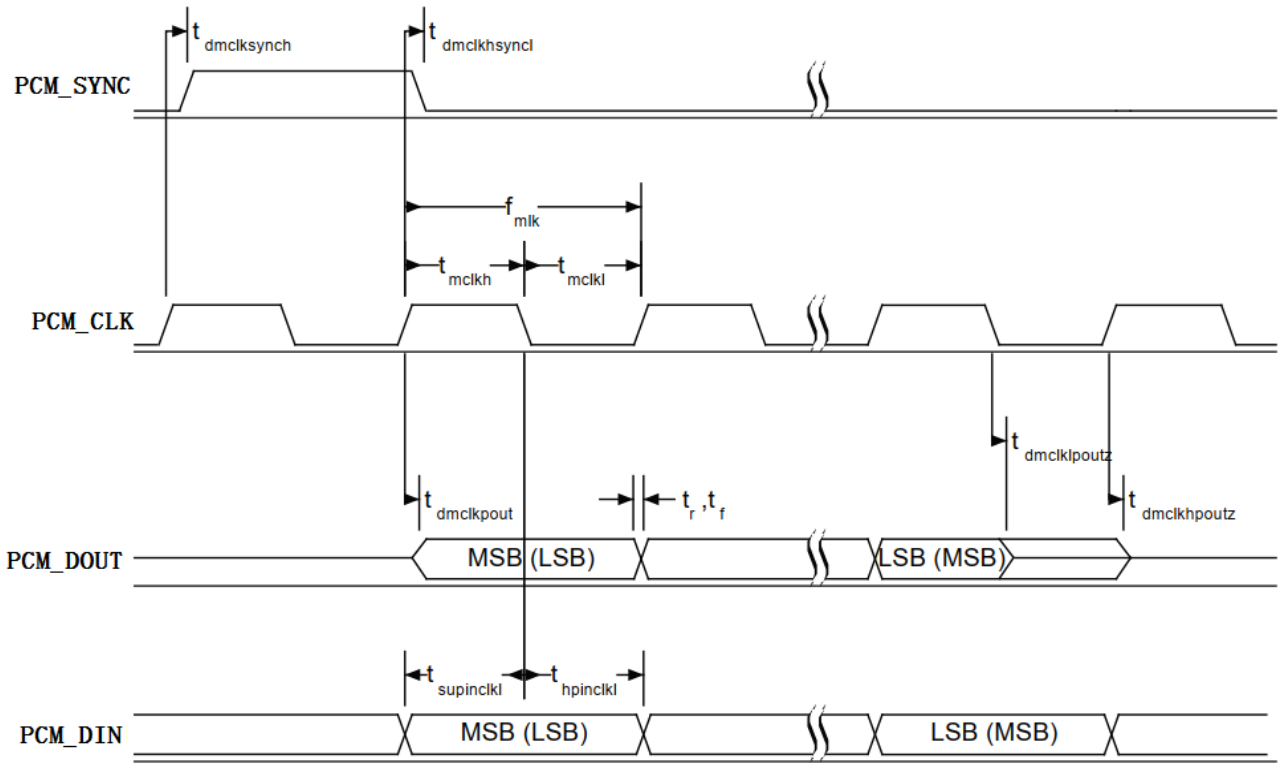

Figure 5: PCM Master Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	-	-	20	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	ns

Table 3: PCM Master Mode Timing Diagram Symbols

5.2.2 PCM Slave Mode Timing Diagram

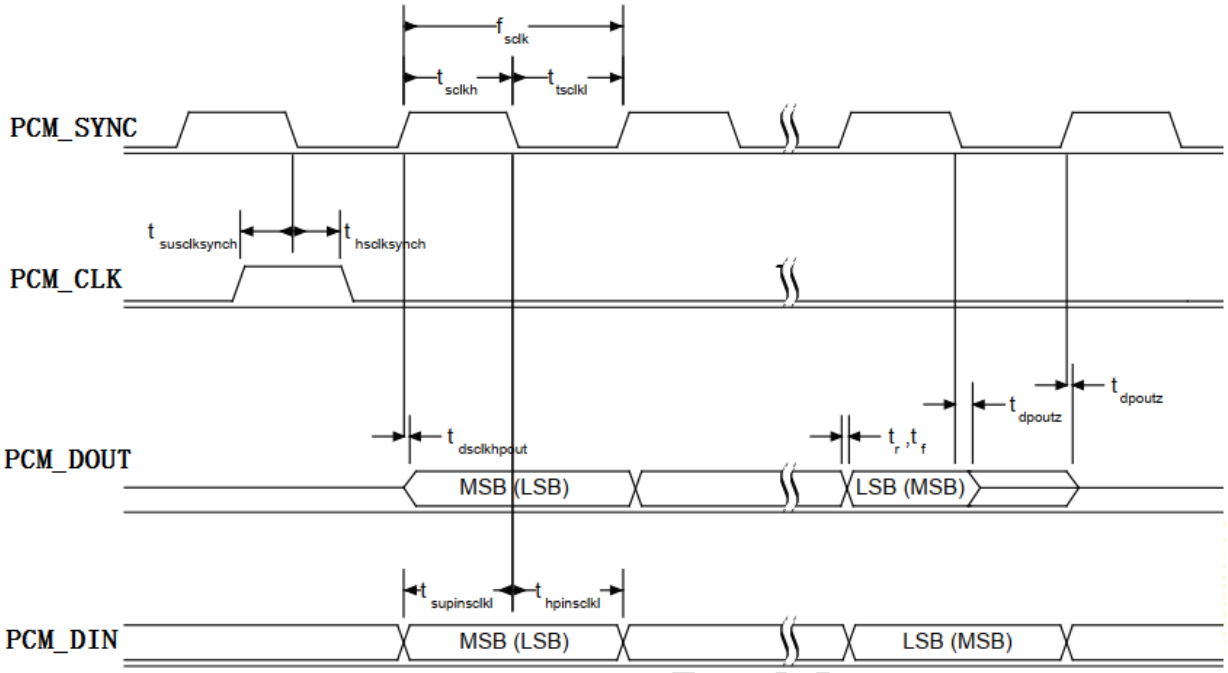

Figure 6: PCM Slave Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	5	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	15	-	-	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	15	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	5	-	-	ns

Table 4: PCM Slave Mode Timing Diagram Symbols

5.3 USB Interface

GOC-QF110 has a USB device interface: An upstream port, for connection to a host Phone/PC or battery charging adaptor.
For details software support for USB features, refer to ADK documentation.

5.3.1 USB Device Port

The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically GOC-QF110 enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.
The DP 1.5 k pull-up is integrated in GOC-QF110. No series resistors are required on the USB data lines. GOC-QF110 contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.
Extra ESD protection is not required on VCHG (VBUS) because GOC-QF110 meets the USB certification requirements of a minimum of 1uF, and a maximum of 10 μF being present on VCHG (VBUS).
The VCHG input of GOC-QF110 is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.

5.3.2 USB Charger Detection

GOC-QF110 supports charger detection to the USB BCv1.2 standard.
It provides Data Contact Detection (DCD) using an internal current source, and provides:
■ Detection of standard downstream ports (SDP)
■ Charging downstream ports (CDP)
■ Dedicated downstream ports (DCP)
The voltage on the USB data lines can be read by the 10-bit auxiliary ADC. This allows detection of proprietary chargers that voltage bias USB the data lines.
For USB C type connectors, the LED pins can be used to detect the voltage on the CC line pins to detect the charge current capabilities of the upstream device.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Ratings	Min	Typical	Max
VBAT	2.80V	3.30V	3.50V

Table 5: Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Working Conditions	Min	Typical	Max
Storage temperature	-40℃	/	+85℃
Operating temperature	-40℃	20℃	+85℃
VBAT	3.13V	3.30V	3.46V

Table 6: Recommended Operating Conditions

7. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak Temperature : <260℃
Number of Times : 2 times

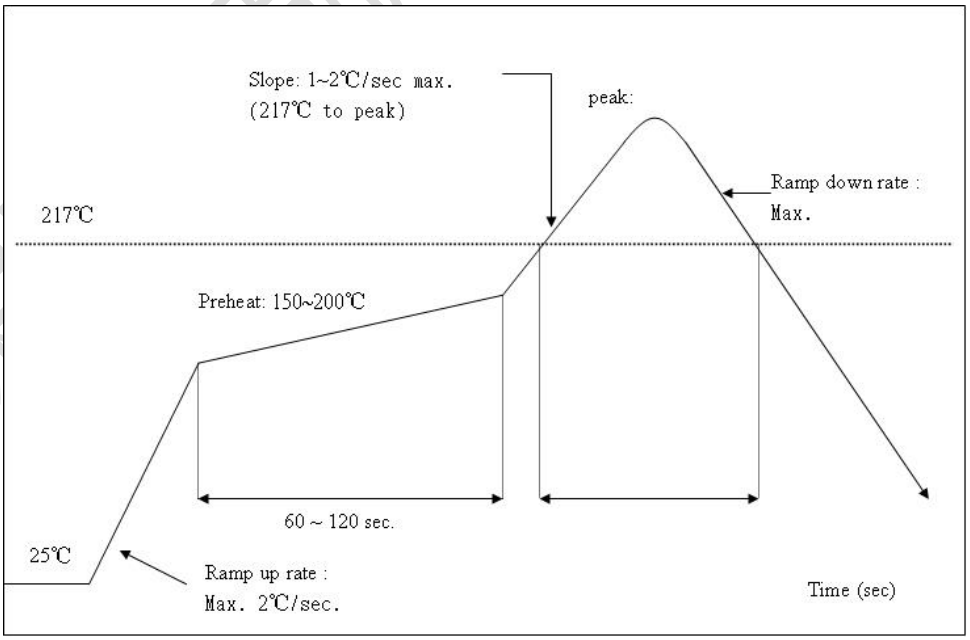

Figure 7: Solder Reflow Profile

8. PCB Layout Recommendation

8.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

8.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA
UART_RX UART_TX UART_RTS UART_CTS
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

8.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA
PCM_SYNC PCM_CLK PCM_DOUT PCM_DIN
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

8.4 Power Trace Lines Layout Guideline

VBAT Trace Width: 30mil

8.5 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.
Add Ground Through Holes to GOC-QF110 Module Ground Pads
Decoupling Capacitors close to GOC-QF110 Module Power and Ground Pads

9. Module Part Number Description

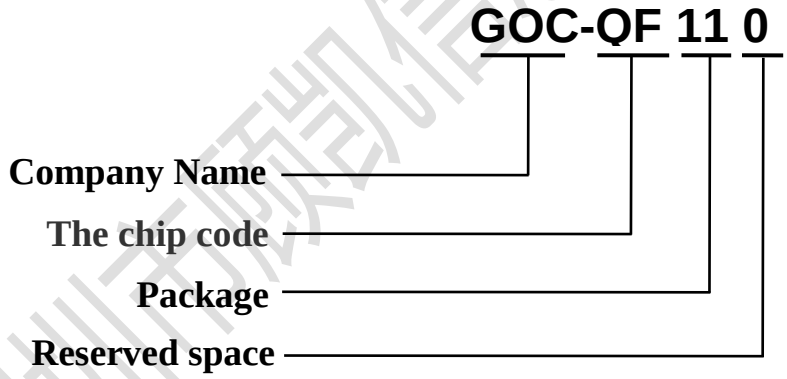

Figure 8: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

10. Ordering Information

Part Number	Description	Remark
GOC-QF110 V1.1	Bluetooth module	

Table 7: Ordering Information

11. Packaging Information

11.1 Net Weight

The module net weight: TBD

11.2 Package

TBD

11.3 Storage Requirements

1）Temperature: 22~28℃;

2）Humidity: <70%（ RH）;

Vacuum packed and sealed in good condition to ensure 12 months of welding.

11.4 Humidity Sensitive Characteristic

1）MSL: 3 level

2）Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3）Handling, storage, and processing should follow IPC/JEDECJ-STD-033